

PATENT

F71989US

"EXPRESS MAIL" MAILING LABEL
NUMBER EL350763114US

DATE OF DEPOSIT 12-20-99

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to:
The Assistant Commissioner of Patents,
Washington D.C. 20231.

Kerry Morris
Signature

See Sub
Spec

APPLICATION FOR LETTERS PATENT

FOR

**ELECTROSTATIC DISCHARGE PROTECTION NETWORK
HAVING DISTRIBUTED COMPONENTS**

Inventors: Dietmar Eggert and Wolfram Kluge

ASSIGNEE: AMD

F71989US

**ELECTROSTATIC DISCHARGE PROTECTIVE NETWORK
HAVING DISTRIBUTED COMPONENTS**

SPECIFICATION

BACKGROUND OF THE INVENTION

5 **FIELD OF THE INVENTION**

The present invention relates to electronic circuits and systems sensitive to electrostatic discharge, and more particularly, to a distributed electrostatic discharge protection network for these electronic circuits and systems operating at radio frequencies.

DESCRIPTION OF THE RELATED TECHNOLOGY

10 Electrostatic charge was discovered by the early Greeks and was a novelty until electricity became better understood and more widely used. An electrostatic charge potential may become so large that the insulation medium between the positive and negative charges breaks down. This break down results in what is called "electrostatic discharge" or "ESD." Examples of minor and major ESD events are an electric spark from a metal door knob to one's finger after shuffling across a carpeted floor, and a lightning bolt between the earth and the clouds, respectively. Electrical and electronic devices and systems are sensitive to ESD because insulation breakdowns, caused by ESD, may seriously degrade the electrical performance characteristics of the device or system. Electrical power systems are protected from ESD (lightning) by protective devices having voltage break down characteristics that 15 short out and dissipate the ESD event before it can damage the electrical system.

20

Electronic circuits and systems have become more susceptible to ESD damage as the circuit elements thereof have become smaller and the insulation thinner therebetween. During the era of vacuum tube technology, the vacuum tube's operating voltages were

hundreds or even thousands of volts, and the spacing between a vacuum tube's elements were fractions of an inch. Today, devices (transistors and diodes) in very large scale integrated circuits typically operate at three to five volts and have element and insulation dimensions of thousandths of an inch (microns). With the micron element spacing of 5 integrated circuit devices, even relatively small ESD events can be catastrophic. The electronics industry has addressed the ESD problem in various ways. One way is to add ESD protective devices into an electronic system so that all input and output lines are clamped below an ESD voltage that would damage the integrated circuits. Using an added ESD protective device, however, does not prevent integrated circuit ESD damage before the 10 protective device is connected to the integrated circuit. Integrated circuit manufacturers have thus tried to incorporate some form of ESD protection into the integrated circuits themselves. Various forms of ESD protective devices such as zener diodes, capacitors and other controlled break down or surge filtering devices have been used to protect integrated circuit 15 input/output ("I/O") lines and typically may be connected between the I/O lines and both power supply rails (V_{DD} and ground). These ESD protective devices, however, have a significant amount of parasitic capacitance (capacitance associated with the structure of the ESD device). This parasitic capacitance may degrade the high frequency signal performance of the I/O lines of the digital integrated circuit that are connected to the ESD protective 20 devices. In addition, the ESD protective devices generally require series resistors, for example, of about 300 ohms in series with each signal path. This combination of significant parasitic capacitance and relatively high series resistance in each of the signal paths of the I/O lines may prevent or impair proper performance of high frequency signals, especially digital signals having very fast rising and falling transition levels, i.e., logic 0 to logic 1, and logic 1 to logic 0, respectively.

What is needed is a system, method and apparatus for electrostatic discharge protection which does not significantly degrade high frequency signal performance.

SUMMARY OF THE INVENTION

The present invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing a system, method and apparatus for electrostatic discharge protection which does not significantly degrade high frequency signal performance. The embodiments of the present invention provide an electrostatic discharge protection network comprising an inductor having at least one turn of a coil, and at least one ESD clamp device connected to the at least one turn of the coil. More than one coil turn may be associated with one ESD clamp device, and more than one ESD clamp device may be associated with one turn of the coil. It is contemplated and within the scope of the present invention that the inductor coil may be comprised of any shape or form, and the ESD clamp device may be, for example but not limitation, a semiconductor device, a gas discharge device, a zener device, metal oxide varistor, avalanche or tunnel diode, or any other type of voltage limiting device.

The inductor portion of the embodiments of the present invention is connected in series between an electronic circuit node being protected and an external signal node which is subject to an ESD event. The ESD clamp device(s) may be connected to the inductor, preferably at each turn of the inductor coil, and to one or both of the common power supply rails. One of the common power supply rails may be at earth ground potential. In addition, it is contemplated and within the scope of the present invention that some of the ESD clamp devices may also be connected between one or more turns of the inductor coil and earth ground.

In the embodiment of the present invention, the series connected inductor coil and parallel or shunt connected ESD clamp devices, having parasitic capacitance associated therewith, form cascaded “ π ” sections of a low pass filter network. The series inductance of the inductor coil preferably cancels out the shunt capacitance of the ESD clamp device(s) 5 connected thereto for signal frequencies below the low pass filter cutoff frequency. Efficient impedance matching for low impedance signal nodes may be accomplished by appropriate selection of inductance and capacitance values for the ESD network of the present invention.

According to an embodiment of the present invention, the ESD protection network is fabricated on a semiconductor integrated circuit substrate, a plurality of turns of a coil are 10 formed from a plurality of conductive layers with a plurality of insulation layers interleaved therebetween. Each one of the plurality of insulation layers having a one of the plurality of conductive layers (forming each coil turn) thereon. Vias are formed in each of the plurality of insulation layers, and conductive material is deposited therein for connecting the plurality of coil turns together to form the inductor. The ESD clamp devices may be formed on each of 15 the insulation layers and attached to the conductive layer coil turns on the insulation layers, or the ESD clamp devices may be formed in the semiconductor substrate as P and N junction wells with connection to the plurality of coil turns made through conductive vias in the various insulation layers on which the conductive layer coil turns are formed thereon.

According to another embodiment of the invention, the ESD protection network is 20 fabricated on a substrate made of insulation material such as ceramic, glass epoxy, a printed wiring board (PWB) and the like. A plurality of turns of a coil are formed on a plurality of insulation layers on the substrate. Each one of the plurality of insulation layers having a one of the plurality of the coil turns thereon. Vias are formed in each of the plurality of insulation

layers, and conductive material is deposited therein for connecting the plurality of coil turns together to form the inductor. The ESD clamp devices may be formed or attached on each of the insulation layers or the ESD clamp devices may be attached to the substrate with connection to the plurality of coil turns made through conductive vias in the various 5 conductive layers the coil turns are formed therefrom.

According to still another embodiment of the present invention, the ESD protection network is fabricated on an non-conductive (insulation) printed circuit board using printed circuit stripline conductors and surface mounted components. The insulation portion of the printed circuit board may be, for example but not limitation, glass epoxy, TEFLON® (a 10 registered trademark of Dupont Co.), ceramic, glass and the like. The printed circuit stripline enables a constant impedance for the signal path. A plurality of turns of a coil are formed on the printed circuit board in a concentric spiral configuration. A metalized via (plated through hole) is formed through the printed circuit board at each of the plurality of coil turns, or portions thereof, and an ESD clamp device is attached to each of these vias and a planar 15 ground plane located on the face opposite the face on which the plurality of coil turns is located thereon. The ESD clamp devices may be connected to the vias and the planar ground plane preferably using surface mount techniques. The plurality of coil turns may be tapped with vias at points of the coil representing a desired inductance needed to cancel out the parasitic capacitance of the associated ESD clamp device. The outer or larger coil turn(s) 20 may be tapped at less than 360 degrees, and the inner or smaller coil turns may be tapped at more than 360 degrees, i.e., a multiple turn.

According to the aforementioned embodiments of the present invention, the insulation layers between the coil turns of the inductor may preferably be very thin so that the turns of

the coil are close together, thus, improving the magnetic coupling therebetween and increasing the effective inductance for a given size coil diameter. It is also contemplated and within the scope of the present invention that a material of high magnetic permeability may be used by locating same within the coil so as to further increase the effective inductance 5 value for a give size of coil structure. This material may be, for example but not limitation, iron oxide, ferrite, or other materials that increase the effective inductance of the inductor coil.

An advantage of the present invention is that signal paths may be protected from an ESD event without causing significant attenuation or degradation of desired high frequency 10 signals.

Another advantage is that parasitic capacitance of an ESD clamp device may be effectively canceled by a series connected inductance.

Still another advantage is attenuation of ESD frequencies above a desired low-pass filter cut-off frequency.

15 A feature of the present invention is fabricating a coil inductor on a semiconductor integrated circuit die by depositing each turn of the coil on a respective insulation layer and connecting the turns together with metalized vias through these respective insulation layers.

Another feature is using vias to connect an ESD clamp device to each turn of the inductor coil.

20 Still another feature is having a constant impedance signal path that protects against an ESD event without significant attenuation of desired signal frequencies.

Other and further features and advantages will be apparent from the following description of presently preferred embodiments of the invention, given for the purpose of disclosure and taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

- 5 Figure 1 is a schematic diagram of a prior art ESD protective circuit;
- Figure 2 is a schematic diagram of an ESD protection circuit, according to the present invention;
- Figure 3 is a schematic orthogonal view of a coil portion of the invention;
- 10 Figure 4 is a schematic elevational cross-section view of an ESD network fabricated on a semiconductor integrated circuit die;
- Figure 5 is a schematic elevational cross-section view of an ESD network fabricated on a substrate;
- 15 Figures 6 and 7 are a schematic plan view and an elevational view, respectively, of an ESD protection network fabricated on a non-conductive portion of the printed circuit board using printed circuit stripline conductors and surface mounted components; and
- Figure 8 is a schematic orthogonal view of the coil portion of Figure 3 and a core having magnetic properties to increase the inductance of the coil.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 1, a schematic diagram of a prior art ESD protective circuit for an integrated circuit is illustrated. An external signal node 104 is adapted for connection to signal circuits external to the integrated circuit package (not illustrated). The external signal node 104 may be for input and/or output signals. An internal signal node 102 is adapted for connection to signal circuits internal to the integrated circuit package. A resistor 106 is connected in series between signal nodes 102 and 104. The resistor 106 may be, for example, 300 ohms. The signal node 104 and the resistor 106 may be connected to ESD clamp devices 108 and 110. The ESD clamp devices 108 and 110 may also be connected to the system's power rails V_{DD} and V_{SS} , respectively. The ESD clamp devices 108 and 110 limit transient voltages coming into signal node 102 to approximately the voltages of the power rails V_{DD} and V_{SS} . A P-channel metal oxide semiconductor (PMOS) transistor and an N-channel metal oxide semiconductor (NMOS) transistor are illustrated for the ESD clamp devices 108 and 110, respectively.

The ESD protection circuit illustrated in Figure 1 is effective but degrades the high frequency performance of desired signals because the ESD clamp devices 108 and 110 have inherent parasitic capacitance and when connected to the resistor 106 form a RC low pass filter that may cause significant attenuation of fast rising digital signals. In addition, impedance matching for optimum signal to noise ratio and/or power transfer is greatly affected when the external signal circuit impedance is much lower than the value of the resistor 106, e.g., 50 ohms. The embodiments of the present invention eliminate the requirement for the series connected resistor 106 and effectively cancel out the undesirable parasitic capacitance at the desired signal frequencies.

The present invention is a system, method and apparatus for providing an electrostatic discharge protection network on an integrated circuit die, a monolithic substrate, and a printed circuit board with or without constant impedance stripline conductors. Embodiments of the invention comprise an inductor having at least one turn of a coil, and at least one ESD clamp device connected to the at least one turn of the coil. More than one coil turn may be associated with one ESD clamp device, and more than one ESD clamp device may be associated with one turn of the coil. It is contemplated and within the scope of the present invention that the inductor coil may be comprised of any shape or form, and the ESD clamp device may be, for example but not limitation, a semiconductor device, a gas discharge device, a zener device, metal oxide varistor, avalanche or tunnel diode, or any other type of transient voltage limiting device.

The inductor portion of the embodiments of the present invention is connected in series between an electronic circuit node being protected and an external signal node which is subject to an ESD event. The ESD clamp device(s) may be connected to the inductor, preferably at each turn of the inductor coil, and to one or both of the common power supply rails. One of the common power supply rails may be at earth ground potential. In addition, it is contemplated and within the scope of the present invention that some of the ESD clamp devices may also be connected between one or more turns of the inductor coil and earth ground.

Referring now to the drawings, the details of preferred embodiments of the present invention are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Referring to Fig. 2, a schematic diagram of the ESD protection circuit of the embodiments of the invention is illustrated. The ESD protection circuit of the present invention is generally represented by the numeral 200 and has an external node 206 and an internal node 208. The external node 206 is adapted for connection to circuits having desired signals with undesirable ESD events and the internal node 208 is adapted for connection to circuits needing protection from ESD events. Between the nodes 206 and 208 The ESD protection circuit 200 comprises a series connected inductor 202 between the nodes 206 and 208, wherein the inductor 202 has tapped portions 202a, 202b, 202c and 202d. Parallel or shunt connected ESD clamp devices represented by their parasitic capacitance 204a, 204b, 202c and 204d are connected to respective inductor 202 tapped portions 202a, 202b, 202c and 202d. The inductor 202 and ESD clamp parasitic capacitance 204 form cascaded “ π ” sections of a low pass filter network. The series inductance of the inductor coil 202 portions 202a, 202b, 202c and 202d preferably cancel out the shunt parasitic capacitance 204a, 204b, 202c and 204d of the ESD clamp device(s) connected thereto for signal frequencies below the low pass filter cutoff frequency. Appropriate selection of inductance 202 and capacitance 204 values for the ESD network 200 may also be used for efficient impedance matching of the signal nodes 206 and 208 to a source and load, respectively.

Referring now to Figure 3, a schematic orthogonal view of an embodiment of the invention is illustrated. The ESD protection network 200 may be fabricated on a semiconductor integrated circuit substrate or any other type of substrate which has insulation thereon (not illustrated). The inductor 202 may be comprised of a plurality of turns formed from conductive layers that are coil shaped. These coil shaped conductive layers, illustrated in Figure 3 as coil turns 202a, 202b and 202c, are formed on a plurality of insulation layers (not illustrated for clarity). Each coil shaped conductive layer is formed on a respective

insulation layer (See Fig. 4). Vias through the insulation layer are used to connect the different coil shaped conductive layers together by conductive connections therethrough (See Figure 4). The shape of the coil may be for example but not limitation, round, square, rectangle, triangle, oval, hexagon, octagon and the like. The conductive layer may be 5 comprised of metal such as, for example but not limitation, copper, aluminum, copper alloy and aluminum alloy, or any other conductive material used in the fabrication of an integrated circuit, such as conductive doped polysilicon.

Referring now to Figure 4, a schematic elevational cross-section view of the ESD network 200 fabricated on a semiconductor integrated circuit die is illustrated. An integrated 10 circuit die, generally represented by the numeral 400, comprises a substrate 410 having doped wells 412a, 412b, 412c and 412d in which ESD clamp devices have either or both PMOS and NMOS transistors formed therein. The PMOS and NMOS transistors of the ESD clamp devices may be connected to the power supply rails, V_{DD} and V_{SS} , in a fashion similar to the PMOS and NMOS transistor connections illustrated in Figure 1.

15 Insulation layer 414d is formed over the substrate 410 and wells 412a, 412b, 412c and 412d. The insulation layer 414d may also be formed over other conducting and insulation layers proximate to the substrate 410. The coil turn 202d is formed over the insulation layer 414d. Similarly, insulation layers 414c, 414b and 414a, and coil turns 202c, 202b and 202a are formed as illustrated in Figure 4. Another insulation layer 416 may be formed over the 20 coil turn 202a for additional circuitry or physical protection of the integrated circuit die.

The ESD clamp devices formed in the wells 412a, 412b, 412c and 412d may be connected to the coil turns 202a, 202b, 202c and 202d, respectively, through conductive vias (holes) in the insulation layers 414a, 414b, 414c and 414d. The vias are filled with a

conductive material such as aluminum. As illustrated in Figure 1, Vias 418a pass through insulation layers 414d, 414c and 414b, and connect the ESD clamp device in the well 412a to the coil turn 202a. The vias 418a do not connect to the other coil turns 202b, 202c and 202d. Vias 418b pass through insulation layers 414d, 414c and 414b, and connect the ESD clamp device in the well 412b to the coil turn 202b. The vias 418b do not connect to the other coil turns 202a, 202c and 202d. Vias 418c pass through insulation layers 414d and 414c, and connect the ESD clamp device in the well 412c to the coil turn 202c. The vias 418c do not connect to the other coil turns 202a, 202b and 202d. Via 418d passes through insulation layer 414d, and connects the ESD clamp device in the well 412d to the coil turn 202d. The internal node 208 connects to circuit logic (not illustrated) of the integrated circuit die, and the external node 206 is adapted for connection to external circuitry. It is also contemplated and within the scope of the invention that the ESD clamp devices may be formed on or attached to each of the insulation layers.

According to another embodiment of the invention, the ESD protection network may be fabricated on a substrate made of either insulation material such as ceramic, glass epoxy, a printed wiring board (PWB) and the like, or conductive material such as aluminum, copper, steel brass and the like. A plurality of turns of a coil are formed on a plurality of insulation layers on the substrate. Each one of the plurality of insulation layers having a one of the plurality of the coil turns thereon. Vias are formed in each of the plurality of insulation layers, and conductive material is deposited therein for connecting the plurality of coil turns together to form the inductor. The ESD clamp devices may be formed or attached on each of the insulation layers or the ESD clamp devices may be attached to the substrate with connection to the plurality of coil turns made through conductive vias in the various insulation layers on which the coil turns are formed thereon.

Referring now to Figure 5, a schematic elevational cross section view of the ESD network fabricated on a substrate is illustrated. A substrate 510 may be non-conductive or conductive. If conductive, an insulation layer 516 may be used, and if non-conductive then no insulation layer 516 may be required. A first coil turn 202a is formed over the insulation layer 516 or over the non-conductive substrate 510. The first coil turn 202a is connected to an external input node 206. An insulation layer 514a is formed over the first coil turn 202a. A second coil turn 202b is formed over the insulation layer 514a. Another insulation layer 514b is formed over the second coil turn 202b. A third coil turn 202c is formed over the insulation layer 514b. Still another insulation layer 514c is formed over the third coil turn 202c. Yet another insulation layer 514d is formed over the third coil turn 202c. A fourth coil turn 202d is formed over the insulation layer 514c. And another insulation layer 514d is formed over the fourth coil turn 202d. The fourth coil turn 202d is connected to an internal node 208. Any number of coil turns and insulation layers are contemplated and within the scope of the present invention.

ESD clamp devices 512a, 512b, 512c and 512d may comprise PMOS and NMOS transistors, and may be connected to power supply rails, V_{DD} and V_{SS} , in a fashion similar to the PMOS and NMOS transistor connections illustrated in Figure 1. It is also contemplated and within the scope of the invention that the ESD clamp devices may be any type of clamp device, connected to a substrate common or earth ground. The ESD clamp devices 512a, 512b, 512c and 512d may be connected to the coil turns 202a, 202b, 202c and 202d, respectively, through conductive vias (holes) in the insulation layers 514a, 514b, 514c and 514d. The vias are filled with a conductive material such as aluminum. As illustrated in Figure 5, Vias 518a pass through insulation layers 514d, 514c and 514b, and connect the ESD clamp device 512a to the coil turn 202a. The vias 518a do not connect to the other coil turns

202b, 202c and 202d. Vias 518b pass through insulation layers 514d, 514c and 514b, and connect the ESD clamp device 512b to the coil turn 202b. The vias 518b do not connect to the other coil turns 202a, 202c and 202d. Vias 518c pass through insulation layers 514d and 514c, and connect the ESD clamp device 512c to the coil turn 202c. The vias 518c do not connect to the other coil turns 202a, 202b and 202d. Via 518d passes through insulation layer 514d, and connects the ESD clamp device 512d to the coil turn 202d. It is also contemplated and within the scope of the invention that the ESD clamp devices may be formed on each of the insulation layers and attached to the conductive layer coil turns on the insulation layers.

Referring now to Figures 6 and 7, a schematic plan view and an elevational view, respectively, of an ESD protection network fabricated on a non-conductive printed circuit board using printed circuit stripline conductors and surface mounted components is illustrated. It is contemplated and within the scope of the invention that transmission line structures may be used instead of coil shaped structures with the ESD clamp devices. The non-conductive portion of a printed circuit board 610 may be, for example but not limitation, glass epoxy, TEFLON® (a registered trademark of Dupont Co.), ceramic, glass and the like. The printed circuit stripline enables a constant impedance for the signal path. A plurality of turns of a coil 602 are formed on the printed circuit board 610 in a concentric spiral configuration. Conductive vias 612a-612d (plated through holes) may be formed through the printed circuit board 610 at each of the plurality of coil turns, or portions thereof. ESD clamp devices 604a-604d may be attached to respective ones of these vias 612a-612d and to a planar ground plane 712. The ground plane 712 may be located on the face opposite the face on which the plurality of coil turns 602 is located thereon. The ESD clamp devices 604 may be connected to the coil turns 602 by vias 612, and to the planar ground plane 710 by vias 608, or, preferably, by using surface mount techniques. The plurality of coil turns 602 may be

tapped with, for example, the vias 612 at points along the coil 602 which may represent a desired inductance needed to cancel out the parasitic capacitance of the associated ESD clamp devices 604. The ESD clamp devices 604 may connect to the outer or larger coil turn(s) at less than 360 degrees, and the inner or smaller coil turns 602 at more than 360 degrees, i.e., a 5 multiple turn.

According to the aforementioned embodiments of the present invention, the insulation layers between the coil turns of the inductor may preferably be very thin so that the turns of the coil are close together, thus, improving the magnetic coupling therebetween and increasing the effective inductance for a given size coil diameter. Referring to Figure 8, a 10 schematic orthogonal view of the coil portion of Figure 3 and a core having magnetic properties to increase the inductance of the coil 202 is illustrated. A core 820 comprising a material of high magnetic permeability may be located within the coil 202 so as to further increase the effective inductance value for a give size of coil structure. This material may be, for example but not limitation, iron, iron oxide, ferrite ceramic, ferrous oxide, or other 15 materials that increase the effective inductance of the inductor coil.

The present invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned, as well as others inherent therein. While the present invention has been depicted, described, and is defined by reference to particular preferred embodiments of the invention, such references do not imply a limitation on the invention, and no such 20 limitation is to be inferred. The invention is capable of considerable modification, alteration, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts. The depicted and described preferred embodiments of the invention are exemplary only, and are not exhaustive of the scope of the invention. Consequently, the

invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.

CONFIDENTIAL